In the specification:

**The paragraph starting at page 1, line 9, is amended as follows:**

Complementary Metal Oxide Silicon (CMOS) technology has played an increasingly important role in the integrated circuit (IC) industry. Over the years, the technology has improved to the point that CMOS technology clearly holds center stage as the dominant VLSI technology. CMOS VLSI technology provides a large number of transistors and input/output (I/O) interfaces on an IC, sometimes called a chip, with extremely high operating speed. These advances in CMOS VLSI technology and especially in fabrication and manufacturing technologies ~~has~~have been driven by the reduction and downsizing of device dimensions.

**The paragraph starting at page 1, line 16, is amended as follows:**

A number of enhancements may be added to the CMOS processes, primarily to increase routability of circuits, provide high quality capacitors for analog circuits and memories, or provide resistors of variable characteristics. Such enhancements includes providing two or more metal layers~~,~~ or double or triple polycrystalline layers. Notably, present technology provides seven or more layers of metal which can be used as signal and power routing layers. These additional layers ease the routing of signals between modules and improves the power and clock distributions to modules. Improved routability is achieved through additional layers of metal or by improving the existing polysilicon interconnection layer.

**The paragraph starting at page 2, line 3, is amended as follows:**

Contacting a first metal layer to a second or higher level metal layer is achieved by a via. When a further contact to diffusion or polysilicon is required, a separation between the via and the contact cut may be required. To do so, a first level metal tab is used to bridge between the second layer metal and the first layer metal. Processes typically require metal borders around a via on booth level of connection to metal layers. These metal borders assure proper connection to the metal layer and avoid potential intermittent contacts.

**The paragraph starting at page 2, line 9, is amended as follows:**

Most ICs with a large number of transistors and extremely high operating speed with a large count of I/O signal interfaces are subject to ~~suffer from~~ core power supply voltage IR drops, if ~~it is~~they are not handled and measured properly. Note here that "I" corresponds to current and "R" corresponds to resistance. A product of I and R yields the resulting voltage drop associated with the current and resistance. The term IR~~, however,~~ is used in the art, however, as it ~~puts~~ draws a designer to consider in the mind of considering both current and resistance effects in reducing supply voltages in an IC. The ~~reduction and~~ downsizing of device dimensions results in increased performance , reduced cost and increased life cycle.~~,~~ ~~however~~However, such ~~reduction and~~ downsizing makes IR drops even more of a concern as it is critical that power to the IC is maintained stable and within very narrow range. In a typical IC situation, the number of I/O interfaces is fixed~~, however,~~ the power consumption and heat generation increases due to the increased functionality and its associated increases in transistors. Moreover, Undesirable IR drops become even more serious in law-voltage supply applications. For example, where an IC is operating at 1.8 volts, even a small IR drop can cause the IC to fail. ~~Moreover~~Then, even a noisy power supply can cause the IC to fail for such a low operating voltage.

**The paragraph starting at page 2, line 29, is amended as follows:**

These and other objectives are achieved in the present invention by providing power to an integrated circuit using a power bus and strips formed on input/output (I/O) pads such a data I/O and multi-level voltage I/O pads. In an exemplary embodiment of the invention, an integrated circuit is disclosed which comprises a power supply I/O pad and a data I/O pad which are made of a deposited conductor. The deposited conductor is typically a metal such as aluminum (Al), tungsten (W) or other conductors known in the art. The power supply I/O pad is connected to a power bus and the data I/O pad is connected to circuitry within the integrated circuit. Moreover, a strip of deposited conductor is formed ~~closely~~ substantially adjacent to the data I/O pad wherein the strip of conductor is connected to multiple points on the power bus. In this manner, multiple parallel paths are developed within the integrated circuit to distribute power within the circuit. In another embodiment of the invention, a similar approach is taken with respect to multi-level voltage I/O pads.

**The paragraph starting at page 3, line 22, is amended as follows:**

The present disclosure ~~describes~~ provides an integrated circuit having an improved power bus with reduced IR drops in the supply power to the integrated circuit. Moreover, the present invention provides a power bus that reduces noise on the power bus itself. Advantageously, manufacturability, testability and reliability are not compromised in the power bus of the present invention. These and other advantages will be clear upon understanding of the drawings and detailed description below.

**The paragraph starting at page 3, line 32, is amended as follows:**

Figure 1 is a cross-sectional view of a semiconductor device illustrating a multiple layer integrated circuit ~~according to an exemplary embodiment of the invention~~;

Figure 2 is a top-view diagram of a packaged integrated circuit along with its input/output structures ~~according to an embodiment of the invention~~;

Figure 3 is a diagram of a metal layer layout used to form ~~busses~~ buses from the data pads and multi-level voltage pads according to an embodiment of the invention;

Figure 4 is a diagram of a metal layer layout for a power bus using multiple metal layers according to an embodiment of the invention; and

Figure 5 is a legend depicting metal layer representations for a seven-layer metal layout with power buses according to an embodiment of the invention.

**The paragraph starting at page 4, line 11, is amended as follows:**

New microprocessors, sometimes called central processing units (CPUs) are continually being developed with higher clock frequencies and increased functionality. Illustratively, reduced instruction set computing (RISC) architectures introduced complexities into interconnect and packaging systems where the input/output (I/O) timing issues at high clock frequencies need to be addressed. ~~With regard to d~~Dynamic random-access memory (DRAM), static random-access memory (SRAM), and electrically programmable read-only memory (EPROM) devices with increasing memory capacity and decreasing data access times are keeping pace with the rapid microprocessor development. In large part, it has been these microprocessors and memories that have driven IC device technologies. The rate of introduction of these IC components has increased over recent years as competition between

manufacturers intensifies. Early introduction of new IC products enables system manufacturers to evaluate the capabilities of these IC components in their own systems. This gives system manufacturers an early start to market their systems with new features to satisfy market demands. To meet the speed/performance challenge, complementary metal-oxide semiconductor (CMOS) device technology is transitioning into newer technologies such as bipolar CMOS (BiCMOS). This technology is a combination of CMOS and bipolar device technologies. In order to meet the challenges of increased speed and functionality, design and process technologies have migrated to sub-micron technologies.

**The paragraph starting at page 5, line 3, is amended as follows:**

Propagation delays due to parasitic capacitances from interconnects are one of the main causes for compromising speed performance in advanced ICs as interconnect dimensions are scaled down. Moreover, increases in die size ~~make~~ increase interconnect lengths ~~very long~~significantly, which results in higher interconnect resistance and capacitance. These very long interconnect lengths provide undesirable IR drops that reduce supply voltages to the IC circuitry and especially core IC circuitry. Innovations in design techniques and the use of electrically superior interconnect and dielectric materials are needed to reduce propagation delays and IR drops.

**The paragraph starting at page 5, line 11, is amended as follows:**

Interconnect layouts reflect a designer's skill in manipulating available die area by using design rules and packing density to connect all necessary components on a die. Predesigned and tested circuit building blocks and powerful computer-aided design (CAD) tools help reduce design effort and expedite turnaround of designs for manufacturing. Algorithms are written to determine the best routing scheme for interblock and intrablock connections. Interconnect layout design is done within the framework of design rules formulated for a given device. These design rules ensure that products are functional within the limits specified. The product and process requirements must be balanced when defining design rules for products. Feedback from process development, manufacturing, and reliability groups is constantly sought to ensure design rules are not violated. If design rules are violated due to process margins then the implications need to be carefully evaluated.

**The paragraph starting at page 6, line 2, is amended as follows:**

Integrated circuits can be divided into three areas including active regions, isolation regions, and interconnects. The present invention involves the inter-layer and intra-layer connection of metals deposited in layers within an integrated circuit. Within the active regions, an integrated circuit comprises transistors and other active devices grown on a semiconductor wafer. In order to make a functional circuit, it is important to connect various transistors and other active devices to each other in a predetermined manner. Figure 1 is useful to gain an understanding of how semiconductor devices are grown on a semiconductor wafer and are connected using multiple layers of metals. As shown in Figure 1, a number of semiconductor devices shown within box 102 have been grown on a semiconductor wafer; this area is part of the active region. Shown within box 102 are semiconductor devices 103a-d. Semiconductor devices 103a-d are grown on a semiconductor wafer using deposition techniques known to those of skill in the art. Each dielectric layer 116, 118, 120 and 122 is planarized to improve lithography and metal step coverage; these dielectric layers are part of the isolation region. Contacts 110 and vias 112, and 114 are opened in the dielectric layers and filled with a metal. In some implementations the vias are filled with tungsten (W) or Aluminum (Al), however, other metals are also appropriate. The metal layers comprise a stack of films ~~as~~ with each layer ~~has~~ having a specific application ~~since~~ as no single layer can effectively satisfy all the stringent requirements for interconnect metalization. Metal contacts are deposited as a first layer of metal designated M1 104 in Figure 1. Similarly, a second layer of metal M2 106 is deposited; finally, a third layer of metal M3 108 is deposited. It is the top layer, in this case the third layer, that is exposed to form pad 124. ~~that~~ This pad 124, is subsequently used for placing bond wires which are in turn connected to package leads. As is known in the art, a barrier metal layer (not shown) is sometimes needed to prevent the aluminum from interacting with adjacent layers. Moreover, to reduce reflectivity of the metal layers, an antireflective coating (ARC) layer (not shown) is also used. If an ARC layer is not used, the highly reflective metal surface will distort ultraviolet (LTV) light which is typically used during a resist exposure process. This distortion can lead to bridging resist material and further lead to poor critical dimension control. Although the cross-sectional example described for Figure 1 is limited in certain respects, one of skill in the art will understand

how the three layer example shown with one bonding pad 124 can be extended to more layers of metal. For example, present technology is currently using upwards of seven (7) metal layers.

**The paragraph starting at page 7, line 6, is amended as follows:**

As CMOS technology migrates to submicron dimensions, we see some inherent limitations due to scaling becoming more important. Although device technologies have been scaled, power supplies are not similarly scaled because of increased system requirements. When the operating voltages are not scaled, the electric fields increase ~~which causes~~thereby causing reliability problems due to, among other things, ~~what are~~ the so-called hot carriers. The reason these carriers are called "hot" is because the electrons gain a significant amount of kinetic energy and inject themselves into the gate oxide to cause charge trapping. The impact of hot carrier degradation is in the form of transistor threshold voltage instability, gate oxide charging, and latch-up. Migration to lower operating voltages such as 1.8 volts reduces hot carrier problems to some extent, but issues associated with noise margin and drive capability remain. As interconnect and capacitive loads do not scale linearly, the drive current must be increased to gain further speed performance.

**The paragraph starting at page 7, line 19, is amended as follows:**

An ever-present challenge in IC design is to include more transistors on a single chip in order to offer customers a greater set of device features and applications. Downward scaling of feature sizes allows an increase in circuit speed and packaging density. This also decreases power dissipation. There are some notable negative effects of downward scaling on transistor, interconnect, and reliability parameters. These arise when the dimensions are scaled down and operating voltages are not, leading to various short-channel effects. In CMOS circuits, scaling can form parasitic bipolar transistors that may turn on and cause ~~what is called~~ latch-up, which damages an IC.

**The paragraph starting at page 8, line 25, is amended as follows:**

Interconnections serve several functions on an IC and can be divided into two groups. First, local interconnects are used to wire a group of both active and passive elements in close

proximity. Generally, these are thin and densely packed metal lines. Second, global interconnections are used to connect the various circuit elements. It is these interconnections that limit the integrity of the power supply to devices and ~~are to~~ which~~the topic of~~ the present invention is directed. The design rules for each of these considerations are different because of their diverse applications. The interconnections, besides carrying current to the active areas, also serve as an interface to the package metalization. The topmost metal lines that carry the bulk of the power are wider and thicker, thereby reducing resistance. The pitch and length of global interconnects ~~pitch and length~~ are determined by the cell size and the layout required for each cell. Interconnect resistance increases as the length increases and cross-sectional area ~~are~~ is reduced. Moreover, the cross-section of metal lines may be reduced as a result of process variations, causing interconnect resistance to increase. To increase transistor packing density, feature sizes are scaled down and the die size is increased. As the die size increases, so does the length of the global interconnection. Line length ~~also~~ contributes to overall resistance and, accordingly, larger IR drops.

**The paragraph starting at page 9, line 8, is amended as follows:**

Input and output structures, collectively called input/output (I/O) structures, require a large amount of circuit design expertise. An important consideration in I/O structures are pads and pad sizes. A major consideration in determining pad sizes is the minimum size for accommodating a bond wire which will ultimately be attached to the pad. A typical pad size is on the order of 100 to 150 square microns. Pads are typically designed to be "core-limited" or "pad-limited." In core-limited designs, the internal core of the chip determines the size of the chip such that thin pads are required. In such a design, the I/O circuitry is placed on either side of the pad. In a pad-limited design, the I/O circuitry is placed toward the center of the chip.

**The paragraph starting at page 9, line 17, is amended as follows:**

Input/output (I/O) connections on an integrated circuit can be divided into three types: power supply I/Os, multi-level voltage I/Os, and data I/Os. As shown in Figure 2 an integrated circuit (IC) 200 contains a core logic 204 within a typically plastic or ceramic casing 202. Connections which are external to IC 200 are made through pins 206, 208, 210 and 212. As

shown in Figure 2, pins 206 provide the positive power supply to the core logic. This positive power supply is usually called $V_{DD}$. A connection from pin 206 is typically made using a metal trace 214 within IC 200. Moreover, a power bus 216 (not shown) is formed to surround core logic 204. Where core logic 204 needs $V_{DD}$, a connection is made from the power bus 216. Similarly, pins 208 provide the negative power supply to the core logic. This negative power supply is usually called $V_{SS}$. ~~That t~~throughout ~~the within the present~~this disclosure voltages are sometimes described as positive or negative, however, it is important to note that this is done for clarity and convenience. One of skill in the art will understand that the positive and negative voltage being described are relative terms that can describe a voltage potential and can further describe the magnitude (i.e., absolute value) of a voltage potential. Accordingly, one of skill in the art would understand a positive voltage as a high voltage and a negative voltage as a low voltage. These and other variations are well understood by those of skill in the art. So as to prevent cluttering of Figure 2, the negative power bus and its connections are not shown, however, the negative power bus is formed in a similar manner as the power bus. One of skill in the art understands that undesirable IR drops are at their worst at the center of the core logic. Intuitively this makes sense as it is the center of the core logic that is the farthest from the negative and positive power ~~busses~~ buses. Thus, associated resistances are at their highest and necessary current draw is also at its highest.

**The paragraph starting at page 10, line 29, is amended as follows:**

The prior art attempted to reduce IR drops by providing more power supply pins and thereby providing parallel current paths to the core logic 204. The present invention avoids this cumbersome solution and instead makes use of the fact that data I/Os and multi-level voltage I/Os do not need to carry much current such that a narrower I/O pad remains and is fully functional. Although the three types of I/Os carry dramatically different amounts of current, they are allocated similar amounts of metal for their pads. As a solution to the IR drop problem, the present invention forms strips out of the outer portions of the pads for the multi-level voltage I/Os and the data I/Os. These strips are then connected to the positive and negative power supply ~~busses~~ buses used for $V_{DD}$ and $V_{SS}$. As shown in Figure 3, $V_{DD}$ I/O pad 302 is used to provide positive power to the power ~~busses~~ buses 304a and 304b. Moreover, $V_{SS}$ I/O pad 306 is used to provide negative power to the power ~~busses~~

buses 308a and 308b. These connections can be made using methods known in the art. As further shown in Figure 3, data I/O pad 310 is made similarly to $V_{DD}$ and $V_{SS}$ I/O pads 302 and 306, however, data I/O pad 310 can function properly with narrower metal contacts without detrimental effects. Accordingly, the present invention allocates strips 312a and 314a from the data contacts for parallel connections to the power ~~busses~~ buses 304a and 308a, respectively. Recall, that a prior art method of decreasing IR drops was to increase the number of power supply pins. The result of this prior art solution was to provide parallel paths for power to be supplied to the integrated circuit. The strips 312a and 314a just described provide a similar effect but without the need to dedicate more pins to power supply inputs. More pins are therefore available to accommodate increased functionality by allowing more data I/Os. As described, these strips 312a and 314a provide parallel connections between the power ~~busses~~ buses and therefore reduce IR drops at the core logic. Similar strips can be made on the positive and negative multi-level voltage pads so as to provide further parallel paths for the power supplies. These are shown as strips 312b, 314b, 312c and 314c, respectively.

**The paragraph starting at page 11, line 22, is amended as follows:**

Detrimental or undesirable IR drops are further reduced in the present invention by providing a grid-type power bus that intersects at or near the center of the core logic. As shown in Figure 4, a $V_{DD}$ I/O pad 402 connects to a positive power bus 404. The power bus 404 of the present invention differs from the prior art in that it is provided as an intersecting grid of conductive traces 414 and 416. As shown in Figure 4, conductive traces 414 and 416 are formed in a vertical and horizontal manner such that they intersect at or near the center of the core logic shown as area 418 through vias 420. Whereas prior art ~~busses~~ buses provide a sometimes ineffective ring around the core logic, the present invention advantageously intersects at or near the center of the core logic thereby providing a significantly shorter path from the $V_{DD}$ power bus. Accordingly, the associated IR drop is advantageously less ~~that~~ than in the prior art. In an embodiment of the invention, the power bus 404 ~~is provided~~ in the form of the grid is provided with many more intersecting vertical and horizontal traces. Accordingly, the center of the core logic as well as other parts of the integrated circuit are provided with many closely available paths to the $V_{DD}$ power bus 404. In yet another embodiment of the invention,

a similar negative power bus 408 is provided through $V_{SS}$ I/O pad 406 to form a grid. The power strips described for Figure 3 are further shown in Figure 4 as $V_{DD}$ strip 410 and $V_{SS}$ strip 412. As previously described, these strips provide parallel current paths so as to reduce the detrimental or undesirable IR drops.

**The paragraph starting at page 12, line 7, is amended as follows:**

A further advantage of the present invention is that power ~~busses~~ buses 404 and 408 when arranged in parallel demonstrate an increased coupling capacitance. Such increased coupling capacitance is desirable on the power ~~busses~~ buses as it helps to provide cleaner and undistorted power. Further coupling capacitance can be achieved by providing power buses on multiple layers to provide a sandwich type coupling capacitance. For example, as shown on Figure 5, $V_{DD}$ power ~~busses~~ buses can be provided at level 1 metal layer M1 452 and level 3 metal layer M3 456 and $V_{SS}$ power ~~busses~~ buses can be provided at level 2 metal layer M2 454 and level 4 metal layer M4 458. This sandwich-type capacitive effect further improves the integrity of the power supplied to the integrated circuit.

**The paragraph starting at page 12, line 24, is amended as follows:**

It has been found that reliability is improved and errors are reduced when the power ~~busses~~ buses are provided at the lowest metal layers within a multiple layer application. As indicated in Figures 4 and 5, $V_{DD}$ power bus 404 is provided at the second metal layer, ~~M2 454~~M1 452, and the $V_{SS}$ power bus 408 is provided at the first metal layer, ~~M1 452~~M2 454. Other layers are also appropriate, ~~however,~~although embodiments of the invention avoid using the top-most layers (i.e., M7 464 and M6 462) as power ~~busses~~buses. These layers are less desirable when bonding pressure applied at the I/O pads as it may cause shorts or other damage in the top most layers. Importantly, however, the present invention can be practiced on any layer. The guidance provided here relates to observations made by the inventors. Where issues related to wire bonding, applied pressure, and shorts are not a concern, the present invention can be practiced on the top layers. As the technology develops and these problems can be avoided, there is less concern with regard to shorts. Moreover, shorts can be avoided by avoiding metal directly below the pads. Layout and design rules can be specified in this situation to

provide a fully functional circuit while avoiding shorts or other damage.